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MICROSYM COMPUTERS INC.

EIOC Evaluation Board - Rev. A

Specification

October 1 1992

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Specification - EIOC Evaluation Board

1: Description

The EIOC evaluation board, revision A, will allow all possible interface modes of the EIOC to be evaluated. All interface circuitry and connectors required are included on the EIOCEVAL board.

For information on the EIOC itself please refer to the Extended I/O Controller Specification.

This document includes the schematic for the evaluation board, information on how to configure the jumpers, and information on the connectors.

2: Installation

2.1: Oscillator

The frequency of operation for the EIOC is factory set at 3.6864MHz. If you wish you can change the crystal to a different frequency. Refer to the EIOC specification for information on appropriate operating frequencies.

If you wish to use an external clock source then change the clock source jumper as described below.

2.2: Power

During operation a 5V ±10% power supply must be connected to the EIOCEVAL board. Power must be supplied via the MICROSYM INTERFACE BOARD CONNECTOR (P1) or the ECHELON APPLICATION INTERFACE BOARD CONNECTOR (P2). The current requirement will vary depending on what is connected to the EIOCEVAL board, but it will not normally exceed 500mA.

An AGC-1 fuse is installed on the EIOCEVAL board. If blown then replace with a fuse with the same type and rating.

Note that the MC145407 RS232 transceiver chip has on-chip DC-DC voltage converters for the RS232 drivers.

2.3: Jumpers

The EIOCEVAL board must be properly configured for the appropriate interface modes. The jumpers on the board should be set before the EIOCEVAL is turned on.

2.3.1: MMIO MODE

If you are not using the EIOCEVAL board in MMIO mode, then remove MMIO MODE jumper (JP6).

If you are using the EIOCEVAL board in MMIO mode then install MMIO MODE jumper (JP6).

2.3.2: CTS/RDY FUNCTION

This jumper (JP1) should be set to CTS when not using the EIOC in MMIO mode.

It should be set to CTS when using the EIOC in MMIO mode and the EIOC is not configured for READY input required.

It should be set to READY when using the EIOC in MMIO mode and the EIOC is configured for READY input required.

2.3.3: KEYBOARD TYPE

This header (JP5) should not have any jumpers installed if a keyboard or keypad is not being used.

2.3.3.1: Matrix Keypad (1-4 Rows)

JP5 should not have any jumpers installed if the EIOC is configured for a matrix keypad with 4 or fewer rows.

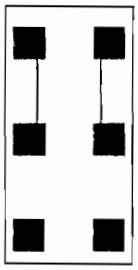
NOTE: in this case make sure that there is no jumper wire installed on P3 (MATRIX KEYPAD) between pins 23 (COL A) and 33 (ROW D).

2.3.3.2: Matrix Keypad (5-16 Rows)

If the EIOC is configured for a matrix keypad with 5 or more rows then jumpers should be installed to short pins on JP5 as follows:

> 4 ROWS

PC A/T



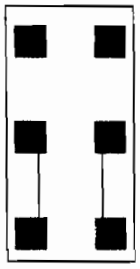
NOTE: in this case make sure that there is no jumper wire installed on P3 (MATRIX KEYPAD) between pins 23 (COL A) and 33 (ROW D).

2.3.3.3: IBM PC/AT Keyboard

If the EIOC is configured for an IBM PC/AT keyboard then jumpers must be installed to short pins on JP5 as follows:

> 4 ROWS

PC A/T



NOTE: in addition to these jumpers, a wire wrap jumper wire must be installed on P3 (MATRIX KEYPAD) between pins 23 (COL A) and 33 (ROW D).

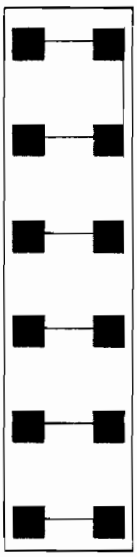
2.3.4: EIOC CLOCK SOURCE

If you wish to use the on-board crystal as the clock source, then the EIOC CLOCK SOURCE jumper (JP2) should be set to Y2.

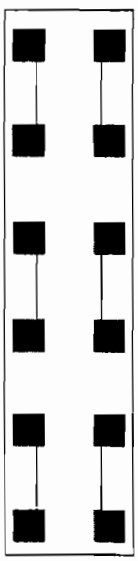
If you wish to use an external clock source (from ECHELON APPLICATION INTERFACE BOARD CONNECTOR P2 pin 2) then the EIOC CLOCK SOURCE jumper (JP2) should be set to P2,2.

2.3.5: DTE/DCE SELECT

If you want the RS-232 connector to be configured as DTE, then install jumpers to short pins on JP7 as follows:

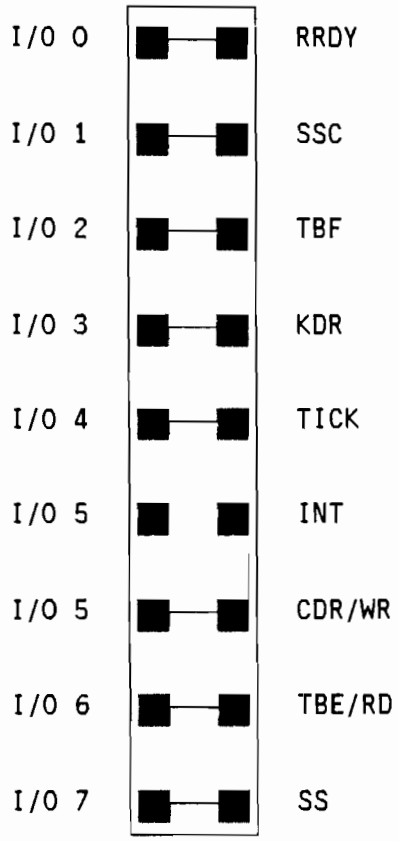


If you want the RS-232 connector to be configured as DCE, then install jumpers to short pins on JP7 as follows:



2.3.6: HOST SIGNALS

This set of jumpers defines which EIOC host signals connect to which I/O signals on the interface board connectors. The HOST SIGNALS jumper block (JP3) with its default jumper positions is detailed as follows:



Note that I/O 5 can be jumpered to either INT or CDR/WR, but it must not be jumpered to both.

Wire wrap jumpers can be used on this jumper block to change the default I/O line connections to the EIOC host signals.

3: Connectors

All interface connectors are described in detail in this section.

3.1: MICROSYM INTERFACE BOARD CONNECTOR

The MICROSYM APPLICATION INTERFACE BOARD CONNECTOR (P1) is wired as follows:

Pin	Signal
1	I/O 0
3	I/O 1
5	I/O 2
7	I/O 3
9	I/O 4
11	I/O 5
13	I/O 6
15	I/O 7
17	I/O 8
19	I/O 9
21	I/O 10
23	+5VDC in
25	+5VDC in
27	+5VDC in
29	+5VDC in
31	+5VDC in
33	-RESET in

All even number pins are connected to ground.

3.2: ECHELON APPLICATION INTERFACE BOARD CONNECTOR

The ECHELON APPLICATION INTERFACE BOARD CONNECTOR (P2) is wired as follows:

Pin	Signal
1	GROUND
2	E (external clock input)
3	GROUND
4	N.C.
5	N.C.
6	GROUND
7	+5VDC in
8	N.C.
9	N.C.
10	-RESET in
11	N.C.
12	N.C.
13	N.C
14	N.C
15	I/O 10
16	I/O 9
17	I/O 8
18	I/O 7
19	I/O 6
20	I/O 5
21	I/O 4
22	I/O 3
23	I/O 2
24	I/O 1
25	I/O 0
26	N.C.

3.3: MATRIX KEYPAD

The MATRIX KEYPAD header (P3) is wired as follows:

Pin	Dir	Signal
1	OUT	COLUMN 1 *
2	IN	ROW 1 $
3	OUT	COLUMN 2 *
4	IN	ROW 2 $
5	OUT	COLUMN 3 *
6	IN	ROW 3 $
7	OUT	COLUMN 4 *
8	IN	ROW 4 $
9	OUT	COLUMN 5 *
10	IN	ROW 5 $
11	OUT	COLUMN 6 *
12	IN	ROW 6 $
13	OUT	COLUMN 7 *
14	IN	ROW 7 $
15	OUT	COLUMN 8 *
16	IN	ROW 8 $
17	OUT	COLUMN 9 *
18	IN	ROW 9 $
19	OUT	COLUMN 10 *
20	IN	ROW 10 $
21	-	NOT CONNECTED
22	IN	ROW 11 $
23	OUT	COL A (GROUND: "column 1" when EIOC is configured for 1 column)
24	IN	ROW 12 $
25	-	NOT CONNECTED
26	IN	ROW 13 $
27	IN	ROW A (1) #
28	IN	ROW 14 $
29	IN	ROW B (2) #
30	IN	ROW 15 $
31	IN	ROW C (3) #
32	IN	ROW 16 $
33	IN	ROW D (4) #
34	-	NOT CONNECTED

* use these column outputs when EIOC is configured for more than 1 column.
$ use these row inputs when EIOC is configured for more than 4 rows.
# use these row inputs when EIOC is configured for 4 rows or less.

3.4: MEMORY MAPPED I/O

The MEMORY MAPPED I/O header (P4) is wired as follows:

Pin	Dir	Signal
1	OUT	A0 *
2	I/O	D0
3	OUT	A1 *
4	I/O	D1
5	OUT	A2 *
6	I/O	D2
7	OUT	A3 *
8	I/O	D3
9	OUT	A4 *
10	I/O	D4
11	OUT	A5 *
12	I/O	D5
13	OUT	A6 *
14	I/O	D6
15	OUT	A7 *
16	I/O	D7
17	OUT	A0/ALE (A0 in non-multiplexed mode; ALE in multiplexed mode)
18	IN	RDY (connects to CTSRDY pin on EIOC via JP1)
19	OUT	GROUND
20	OUT	CS
21	OUT	GROUND
22	OUT	WR
23	OUT	GROUND
24	OUT	RD
25	OUT	GROUND
26	OUT	VDD (+5VDC)

* these address outputs are only available if the EIOC is configured for multiplexed address/data.

3.5: CARD READER

The CARD READER connector (P5) is wired as follows:

Pin	Dir	EIOC Signal
1	OUT	VSS (GND)
2	IN	CD
3	IN	CCK
4	IN	CLS
5	OUT	VDD (+5VDC)

3.6: PROTOTYPE AREA I/O SIGNAL ACCESS

The PROTOTYPE AREA I/O SIGNAL ACCESS connector (P6) is wired as follows:

Pin	Signal
1	I/O 0
2	I/O 1
3	I/O 2
4	I/O 3
5	I/O 4
6	I/O 5
7	I/O 6
8	I/O 7
9	I/O 8
10	I/O 9
11	I/O 10
12	RESET
13	VDD (+5VDC)
14	GROUND

3.7: IBM PC/AT KEYBOARD

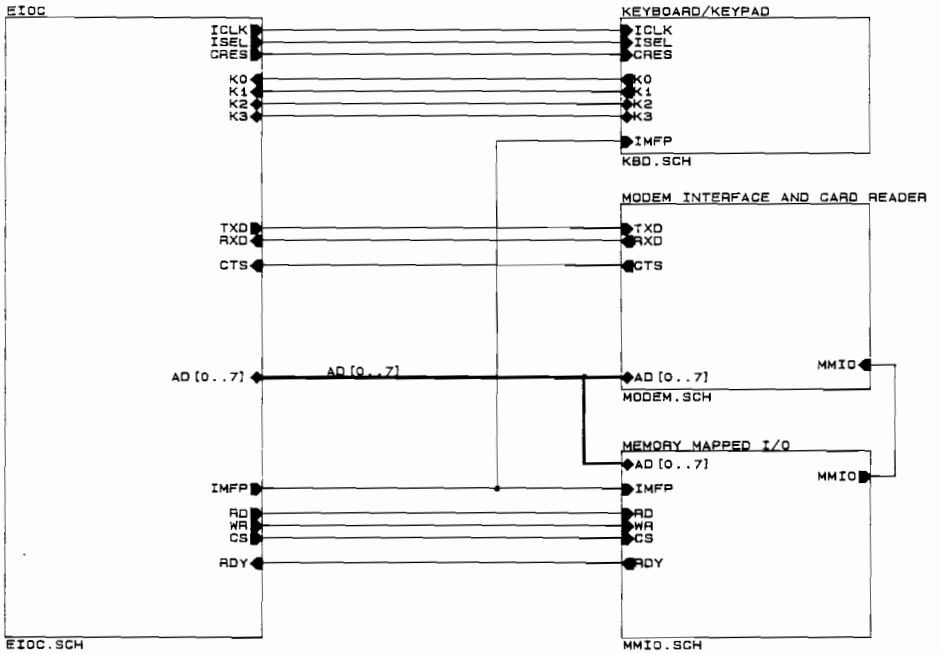
The IBM PC/AT KEYBOARD jack (J1) is wired as follows:

Pin	Dir	Signal
1	I/O	CLOCK
2	I/O	DATA
3	-	NOT CONNECTED
4	OUT	GND
5	OUT	+5VDC

3.8: RS-232

The RS-232 jack (J2) is wired as follows:

Pin	DTE	DCE	Signal
1	-	-	GND
2	OUT	IN	TXD
3	IN	OUT	RXD
4	OUT	IN	RTS
5	IN	OUT	CTS
6	IN	OUT	DSR
7	-	-	GND
8	IN	IN	DCD
20	OUT	IN	DTR
22	IN	IN	RI



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Title
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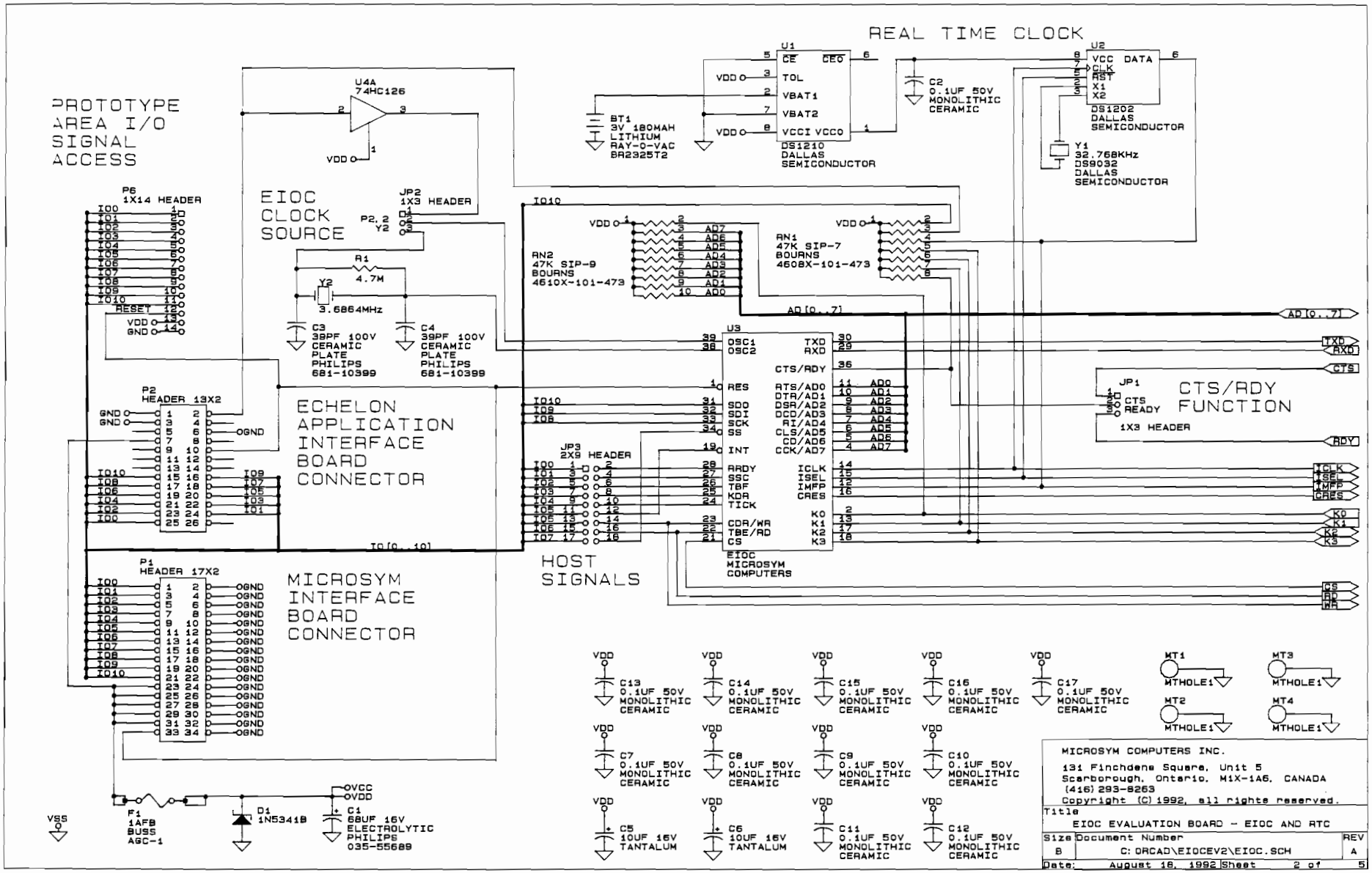
Date: August 18, 1992 Sheet 1 of 5



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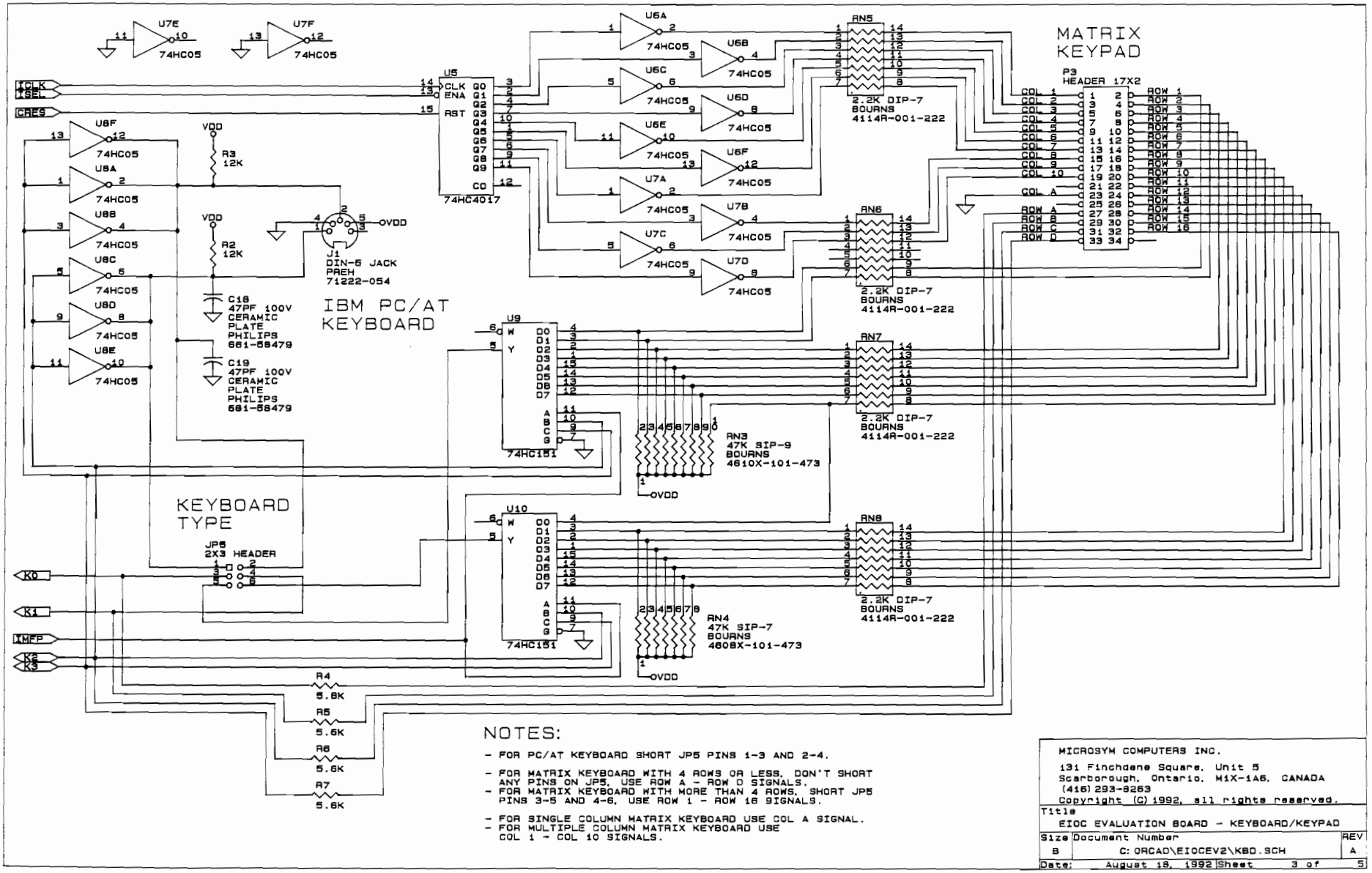

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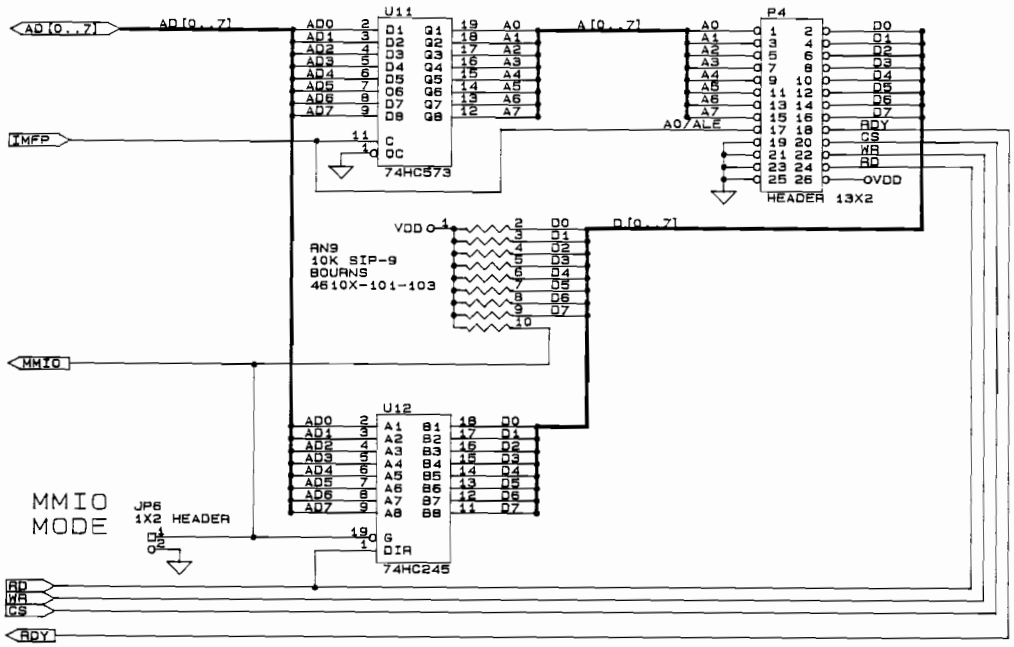
MEMORY MAPPED I/O



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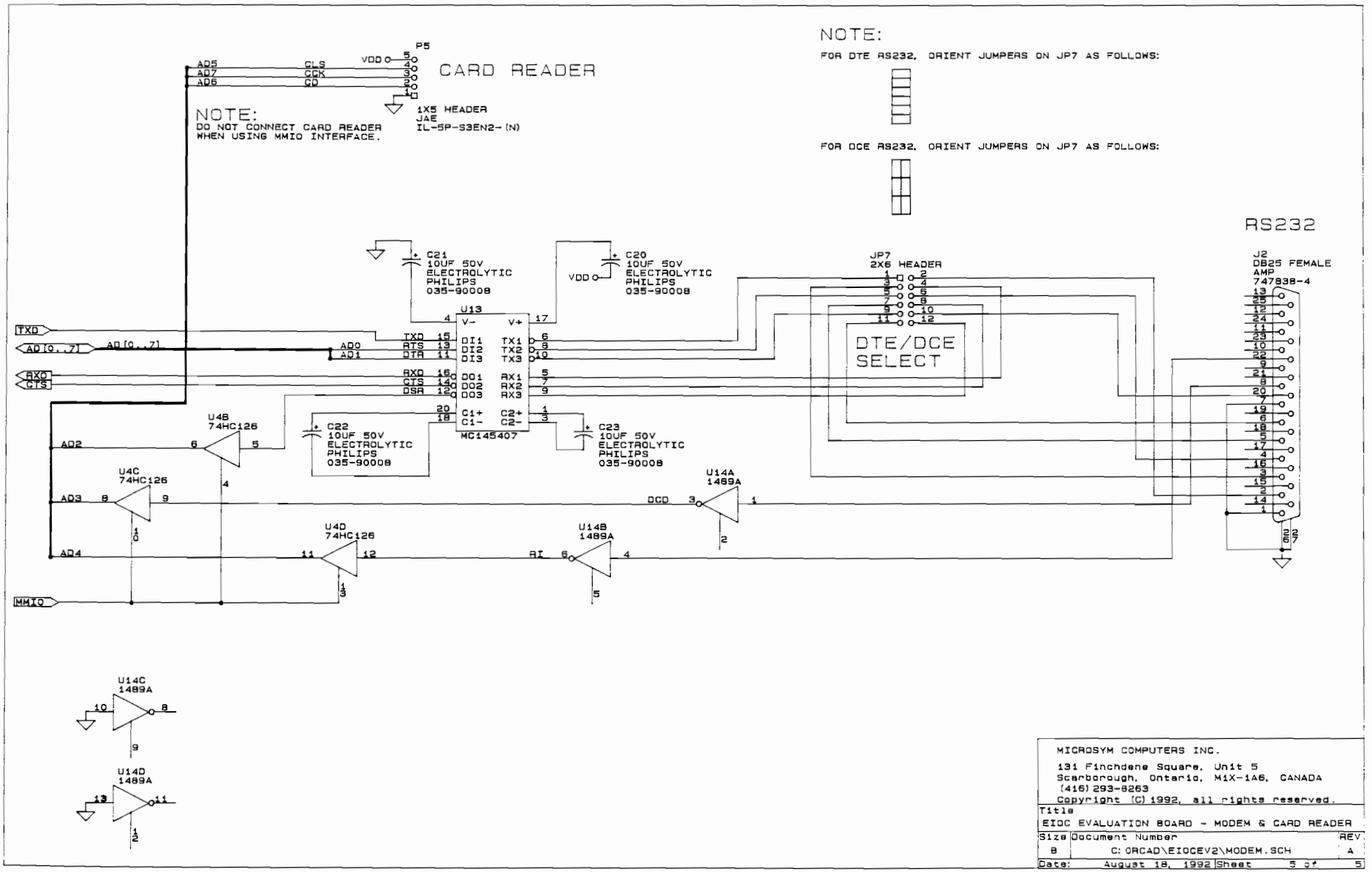

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